

FIG. 1A

FIG. 1B is a block diagram of a system architecture showing memory access and execution rings.

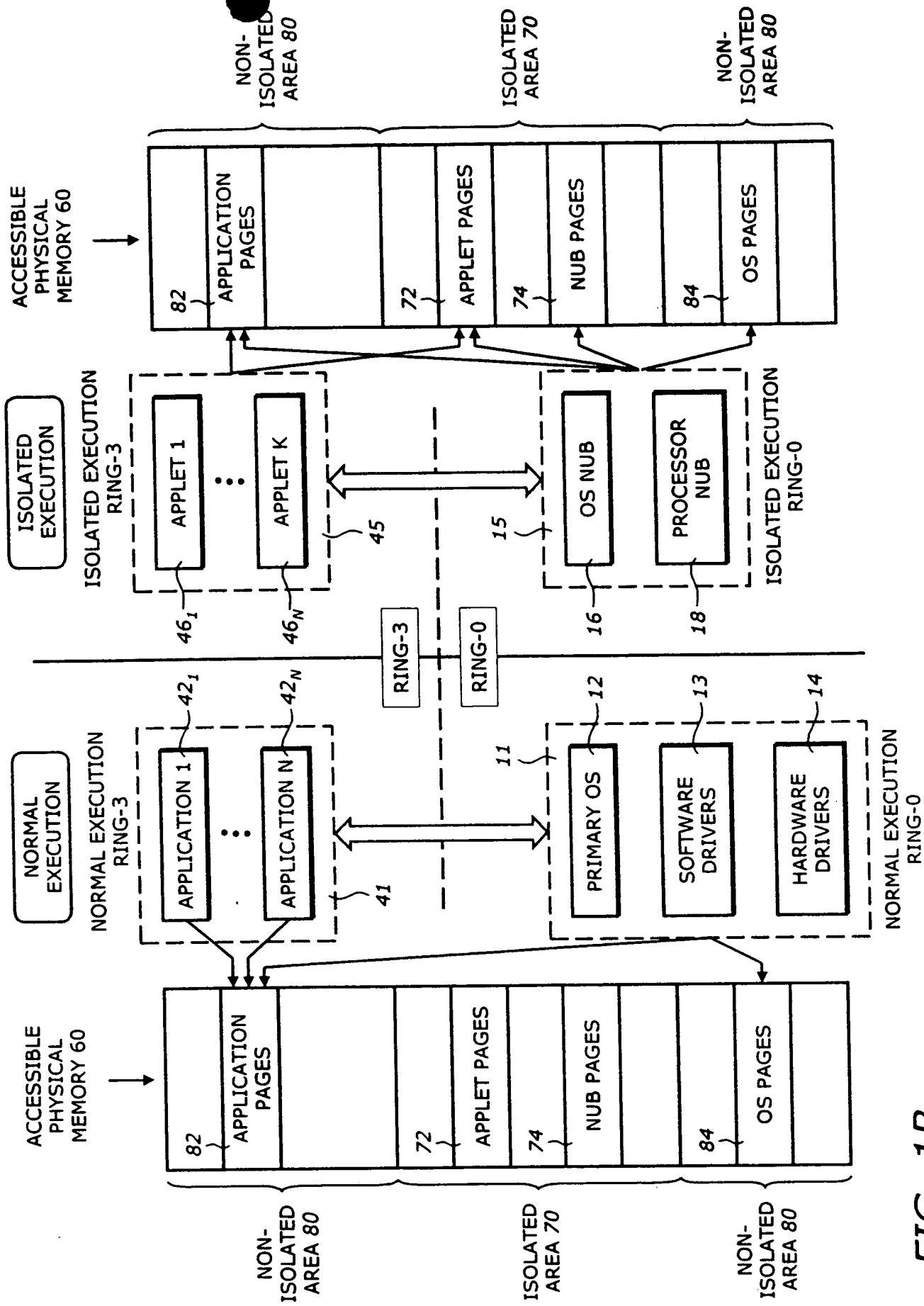


FIG. 1B

100

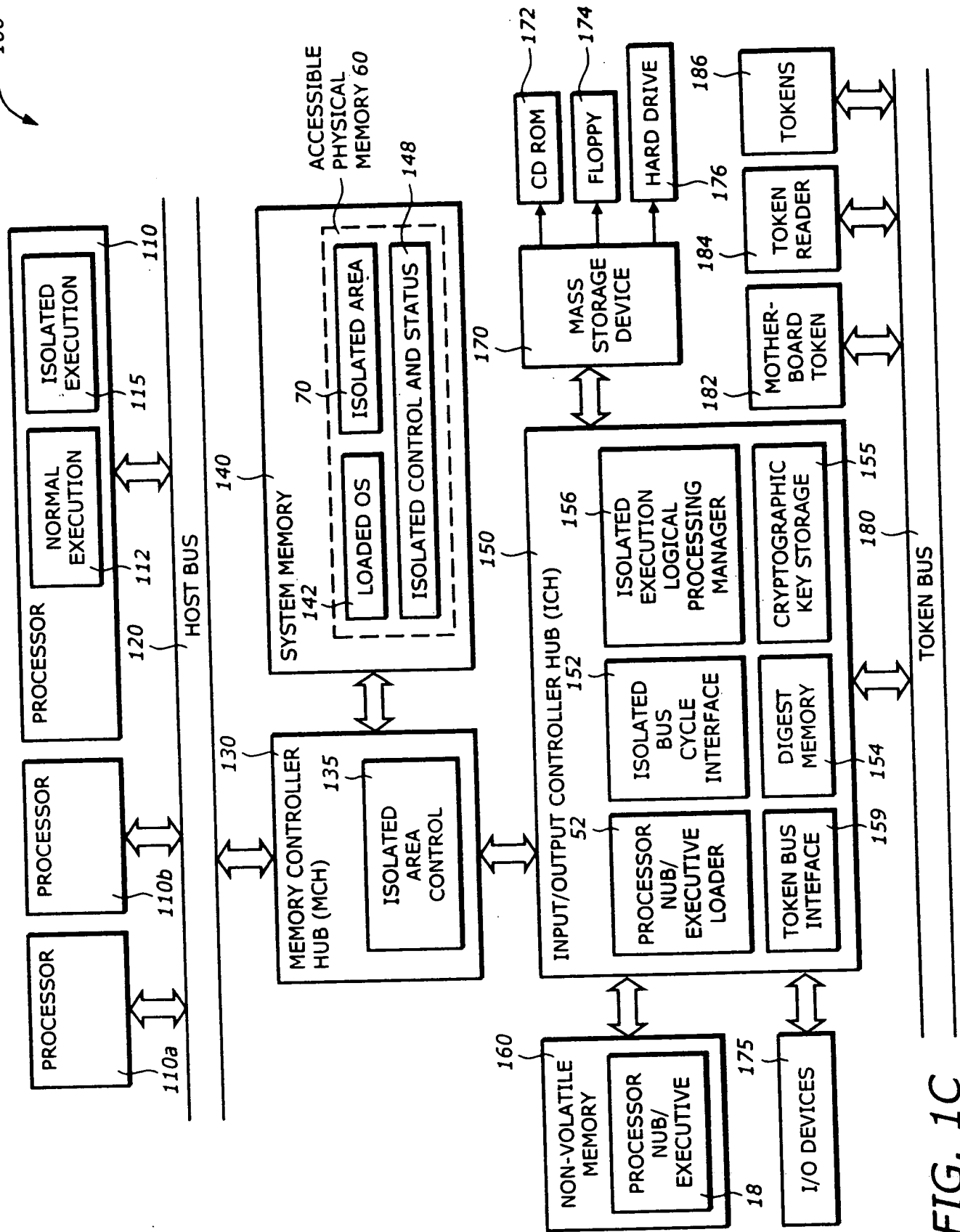
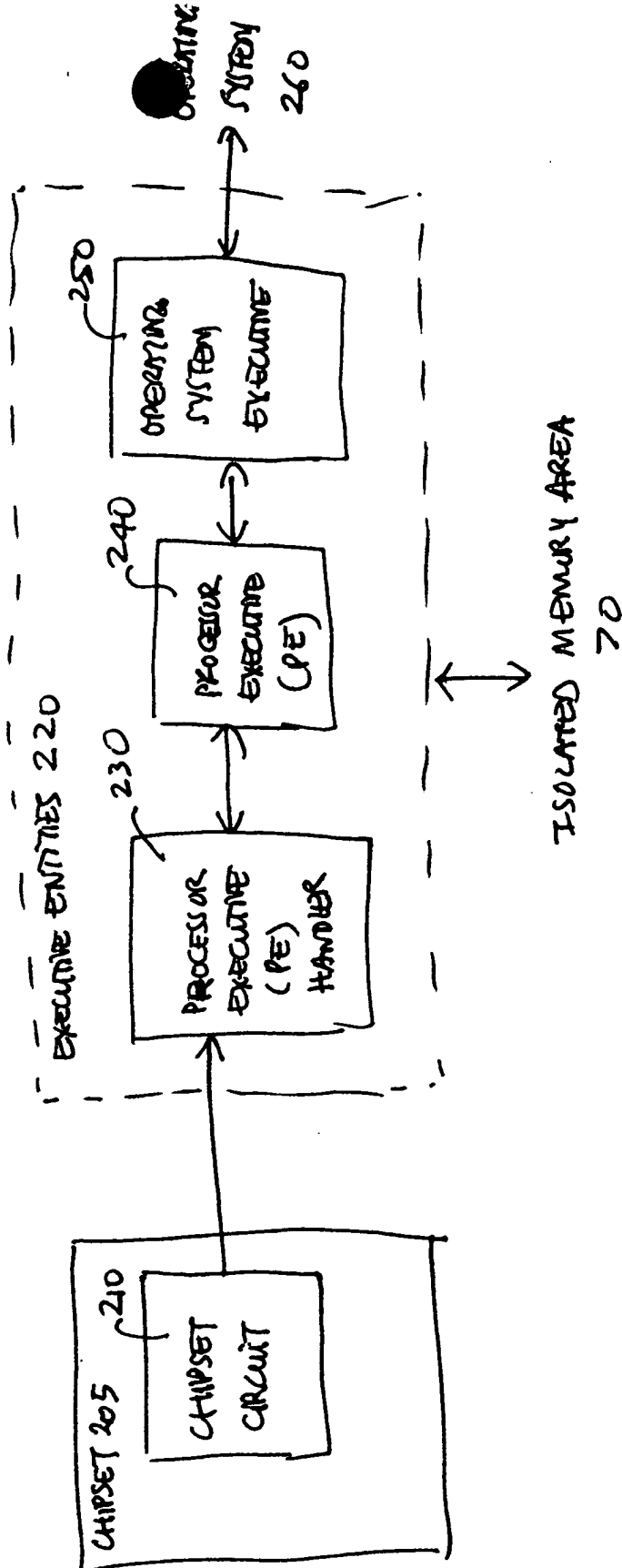


FIG. 1C

200
↓

FIG. 2



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FIG. 2

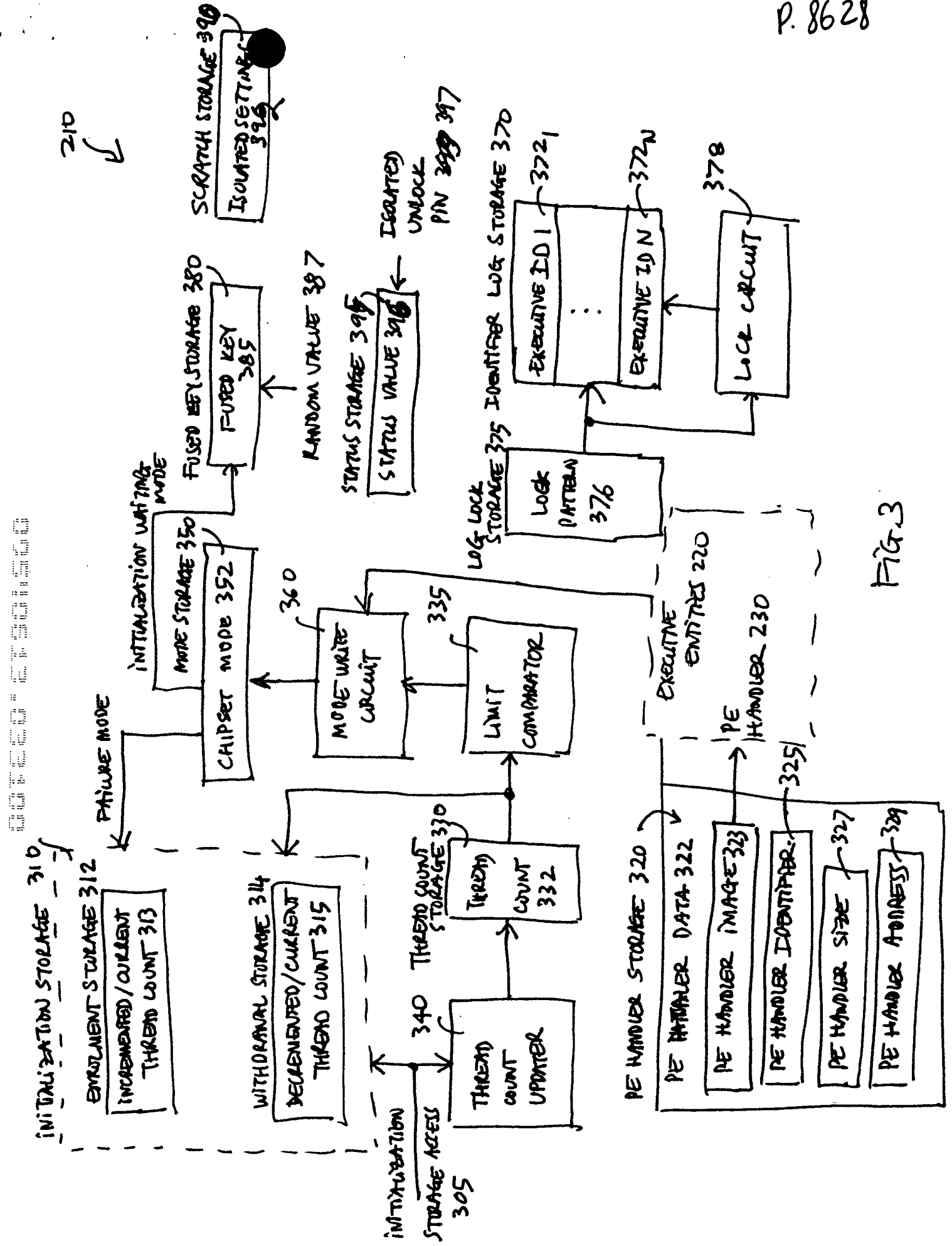


FIG. 3

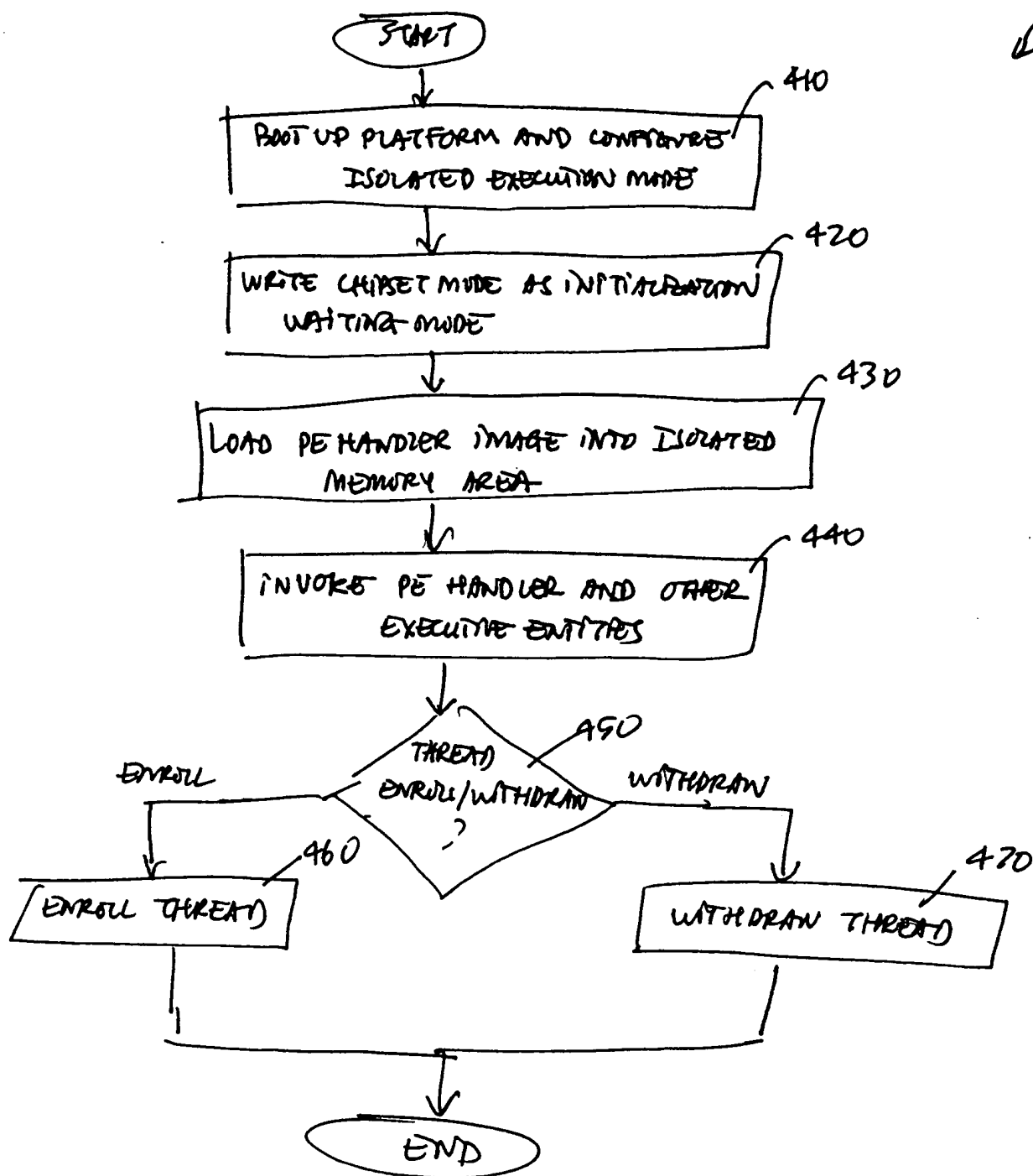


FIG 4

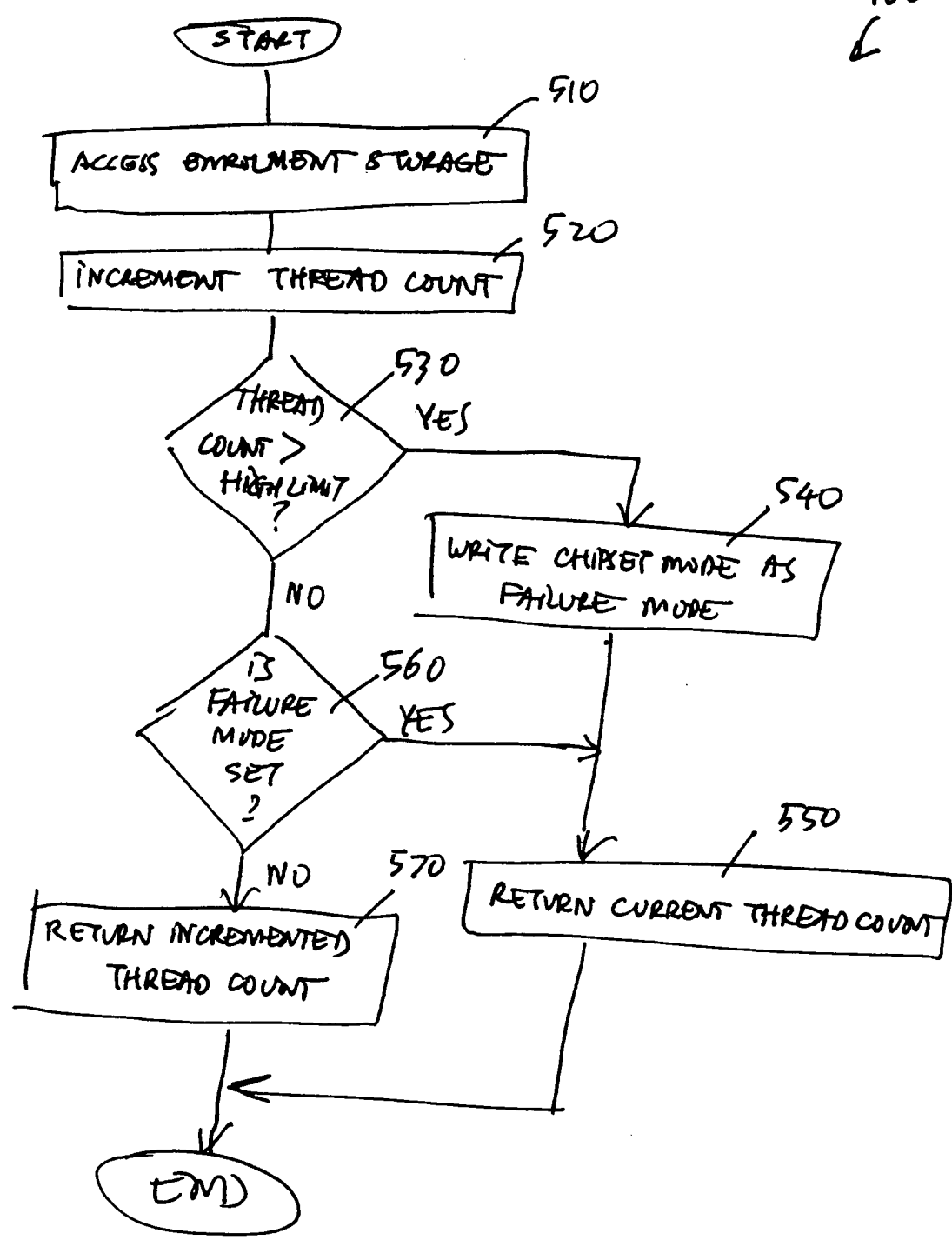


FIG. 5

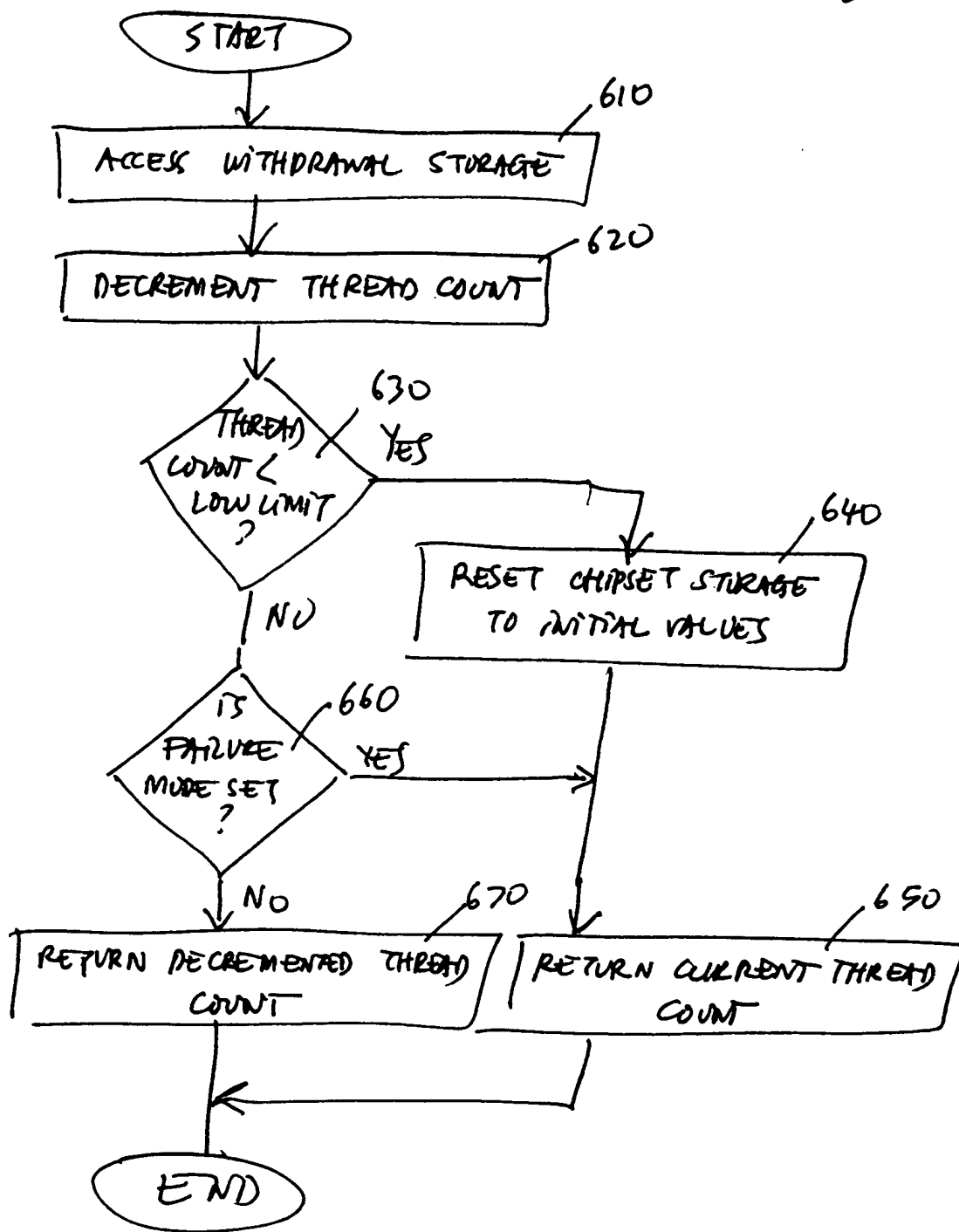


FIG. 6

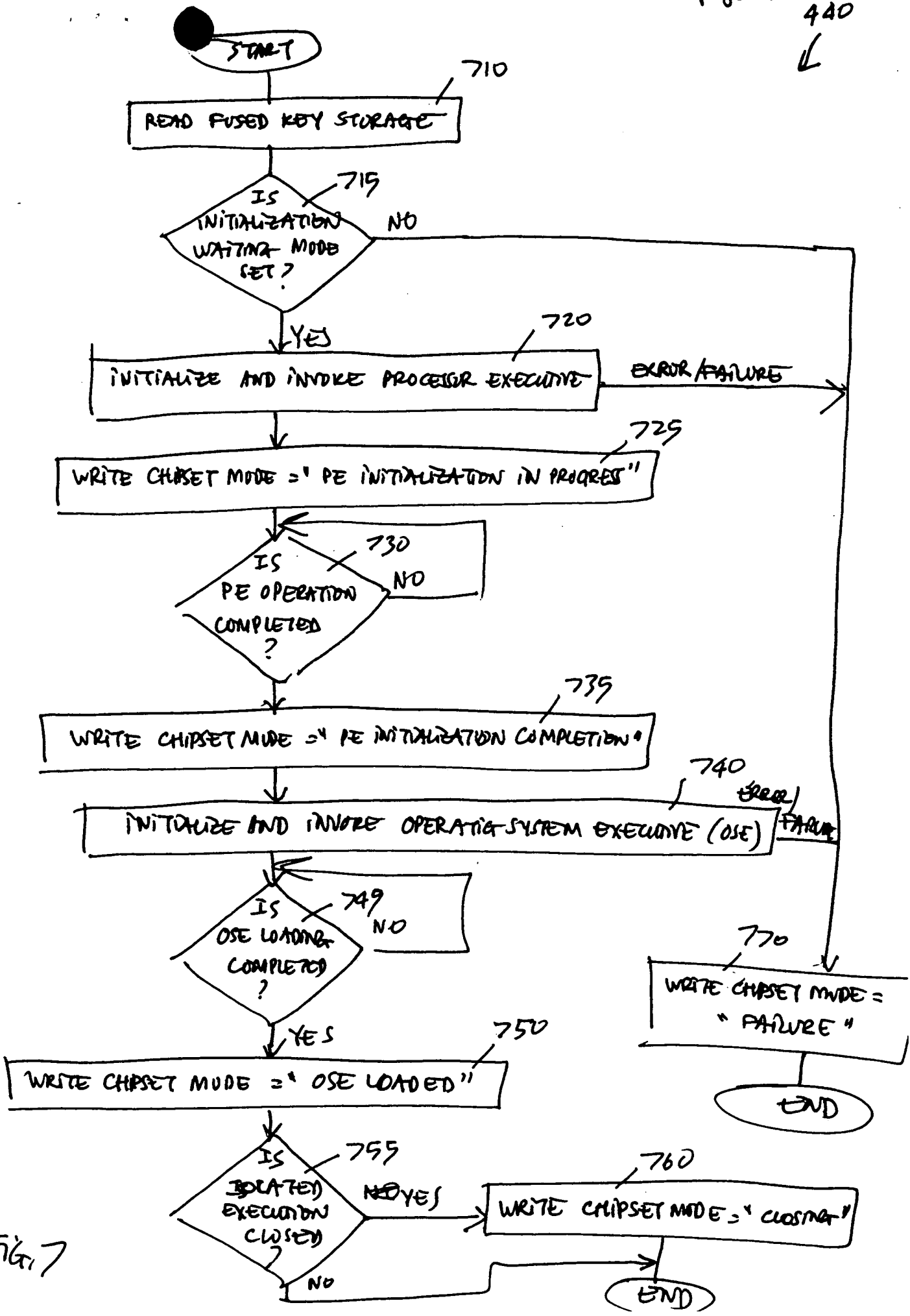


FIG. 7